

- star network topology, 110–111, 217
 - start bit, 45–47, 99, 101, 99
 - state, 18
 - state machine, *see* FSM
 - static electricity, 309
 - status flags
 - ALU, 59
 - subroutine call, 60
 - stepper, *see* photolithography
 - sticky status bit, 232–233
 - stop band, *see* filter
 - stop bit, 99, 101
 - subnet, 195
 - subroutine
 - assembly language, 73
 - defined, 60
 - return-from, 60
 - sum of products, 9
 - PLD, 252
 - superpipelining, *see* pipelining
 - superposition principle, 329
 - superscalar architecture, 163–164
 - switch, network, 194, 218
 - Sylvania, 42
 - synchronizing across clock domains, *see* clock
 - synchronous
 - FIFO interface, 95
 - inputs to flip-flops, 19
 - logic, defined, 21–22
 - reset using Verilog, 226
 - SDRAM interface, 174–175
 - source-synchronous, *see* source-synchronous
 - timing analysis, 23–25
 - Synopsys, 224, 244
 - Synplicity, 244
 - synthesis, *see* logic synthesis
- T**
- TCP (transmission control protocol), 195–196
 - termination, *see* transmission line
 - test
 - design for, 430
 - equipment, 440–442
 - test bench, *see* HDL
 - Texas Instruments, 42, 107, 167, 199, 252, 326, 346, 358, 366, 384, 388
 - thermal analysis, 374–376
 - derating for temperature, 376
 - discrete current regulator, 380–382
 - discrete series regulator, 380–382
 - junction temperature, 375
 - power dissipation, 268, 295, 300, 375–376, 378–379
 - shunt regulator, 378–379
 - thermal resistance, 375, 380
 - timeout, 117, 132
 - timer, 129–130
 - logic design example, 232, 234
 - multitasking, 158
 - prescaler, 232, 234
 - watchdog, 132
 - timing analysis, 23–25
 - clock domain crossing, 233–235
 - clock skew and jitter, 25–27
 - high speed example, 368
 - timing diagram, 19
 - microprocessor read, 66
 - microprocessor write, 66
 - TLB (translation lookaside buffer), 161
 - totem pole output stage, *see* TTL
 - trailer, network, 111, 194
 - transducer, 98
 - transformer
 - common mode filter, 290
 - defined, 288
 - impedance matching, 291
 - placed after rectifier, 297
 - power distribution, 289
 - transistor, 33
 - BJT (bipolar junction transistor), 34
 - BJT beta constant, 300
 - BJT digital amplifier, 301–303
 - BJT logic functions, 304–305
 - BJT operation, 300–301
 - current regulator, 381
 - Darlington pair, 303–304
 - DRAM cell, 88
 - EPROM bit structure, 79
 - FET (field effect transistor), 34
 - FET and static electricity, 309
 - FET digital amplifier, 308
 - FET operation, 306–307
 - FET parasitic properties, 308
 - FET power applications, 309
 - FET, depletion-type, 309
 - flash bit structure, 81
 - JFET (junction FET), 309
 - power dissipation, 300, 303
 - series voltage regulator, 379–382

SRAM cell, 86
 switching regulator, 386–387
 transmission line, *see* signal integrity
 AC termination, 405–406
 characteristic impedance, 398
 defined, 398
 graphical representation, 403
 model, 398
 parallel termination, 403–404
 PCB topologies, 400–401
 reflection coefficient, 399
 reflections, 406–407
 RS-422, 107–108
 series/source termination, 358–359, 406–407
 Spice simulation, 438–440
 termination, 358–359, 403–407
 Thevenin (split) termination, 405
 versus wire, 403
 transport layer, 194–195
 tri-state buffer, 229
 bus expansion, 71
 defined, 29
 memory and microprocessor usage, 65
 versus open-collector, 119
 truth table, 4
 TTL (transistor–transistor logic), 50, 299, 304–305
 totem-pole output, 305
 twisted pair, 197
 two's complement, 16–17

U

UART (universal asynchronous receiver/transmitter)
 data buffer, 100
 defined, 99
 general structure, 100
 handshaking, 99–100
 versus serdes, 199
 unary operator, 4
 underflow, *see* FIFO
 Underwriters Laboratories, 390
 unicast address, 112
 UNIX, 158
 unsigned arithmetic, 14–16
 unused logic gates in schematic diagram, 44–45
 user datagram protocol (UDP), 196
 UV (ultraviolet) light
 EPROM erasure, 79–80
 photolithography, 36

V

VCC, 44–45, 306
 VCO, 362
 Vectron International, 357
 VEE, 306
 Verilog, 222–226
 ? operator, 232
 address decoding logic, 227–228
 always block, 224
 bidirectional signals, 232
 blocking and non-blocking assignment, 225
 case, 228–229, 244
 constants, 225
 continuous assignment, 224
 CPU support logic, 227–233
 default case, 230–231, 239
 finite state machine design, 239–241
 flip-flop, 225–226
 inout, 232
 interrupt logic, 232–233
 latch avoidance, 229
 pipelined FSM design example, 245–247
 posedge and negedge, 225–226
 reg, 222–223, 229
 sensitivity list, 224
 timer design, 232, 234
 wire, 222–223
 VHDL, 222
 via, *see* PCB
 Vicor, 388
 virtual memory
 conceptual cache, 160
 defined, 158
 MMU, 158–161
 page table, 160
 TLB, 161
 working set of memory, 160
 Vishay, 389
 Vitesse, 199
 VLAN (virtual LAN), 217
 VLSI (very-large-scale integration), 39
 volatile memory, 57, 77–78, 86
 voltage
 adjustable linear regulator, 384–385
 characteristics, 373–374
 description, 372
 diode shunt, 377–379
 discrete series regulator, 379–382
 dropout voltage, 373